

Fig. 1

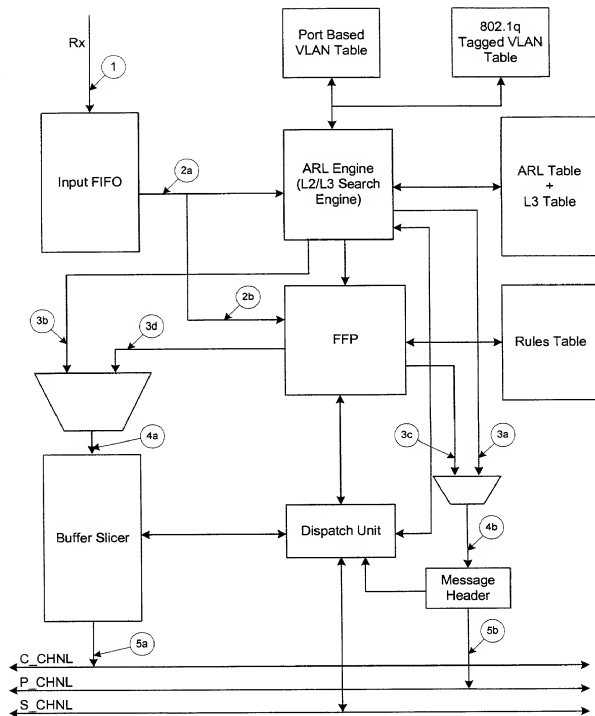


Fig. 2

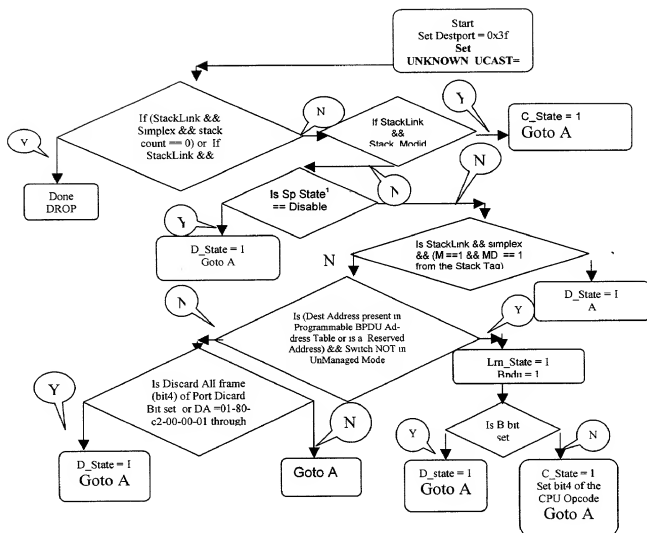


Fig. 3

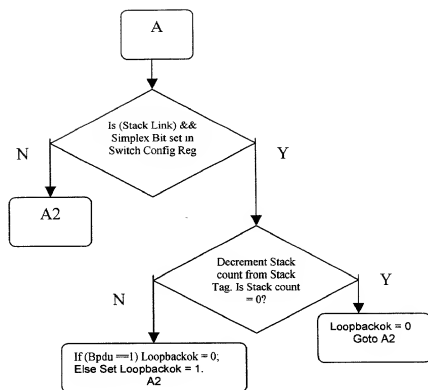


Fig. 4

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graph TD
    A2[A2] --> D1{Is the Pkt Tagged with VID < 1 or packet is Untagged or Switch in}
    D1 -- Y --> B1[Get the VID and PORT_BLOCK_MASK from PTABLE. Use this VID as index into the VTABLE to get STG, VLAN PortBitmap and untagged bitmap, Module Id bitmap.  
if (untagged packet && RPE is set in PVLAN Table), pickup 802.1p from the PVLAN table Modify the packet with new 802.1p  
If (pkt is (tagged or Priority tagged) and Unmanaged mode)  
Set the Untag Bitmap = 0  
If (Pkt is untagged)  
Modify the packet with the VID from PTABLE  
If (pkt is Priority tagged && !Unmanaged mode)  
Modify the packet with the VID from PTABLE  
Use this VID from PTABLE for ARL Src and Dest Lookup, MC Lookup and IPMC Lookup]
    D1 -- N --> D2{If VID=0xffff AND VLAN Id Present in VTABLE}
    D2 -- Y --> B2[Get the STG, VLAN PortBitmap, Untagged bitmap and Module Id Bitmap from VTABLE  
If (StackLink) {  
If (SRC_T) {  
Construct INDEX using Stack_Modid, SRC_T, SRC_TGID)  
Else  
{Construct INDEX using Stack_Modid, SRC_T and Src_Port}  
Get PORT_BLOCK_MASK from the StackMask Table with the constructed INDEX }  
Else  
Get PORT_BLOCK_MASK from the PTABLE corresponding to the Ingress port]
    D2 -- N --> D3{Is C_DROP bit set?}
    B1 --> D3
    B2 --> D3
    D3 -- Y --> B3[Send the Pkt only to CPU  
Get STG(0), Untagged bitmap from PTABLE. Set bit 1 of Cpu Opcodes->C]
    D3 -- N --> D4{Is (Port Discard Bit 5 set) AND NOT (D_State || C_State)}
    B3 --> D4
    D4 -- Y --> D5[D]
    D4 -- N --> D6{Is this port part of VLAN}
    D6 -- Y --> D7{Is enable Ingress Filtering bit set?}
    D6 -- N --> D8[PortBitmap = PortBitmap & DLF Trunk bitmap  
If (C_State)  
If (Lrn_State >= E_Src_Search)  
If (D_State || C_State)  
{ If (C_State) > C;  
else ->D;  
} else {  
E_Src_Search:  
if (Ingress Port in FWD State)  
E_Dst_Search:  
else {  
Increment PortInDiscard  
-> D  
}  
}  
]
    D7 -- Y --> D5
    D7 -- N --> D8
    D8 --> D5
  
```

Fig. 5

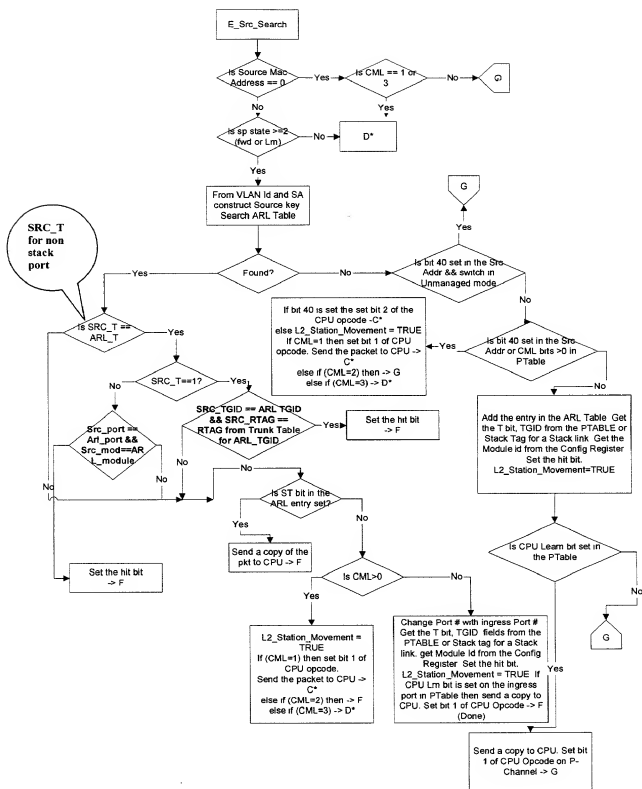


Fig. 6

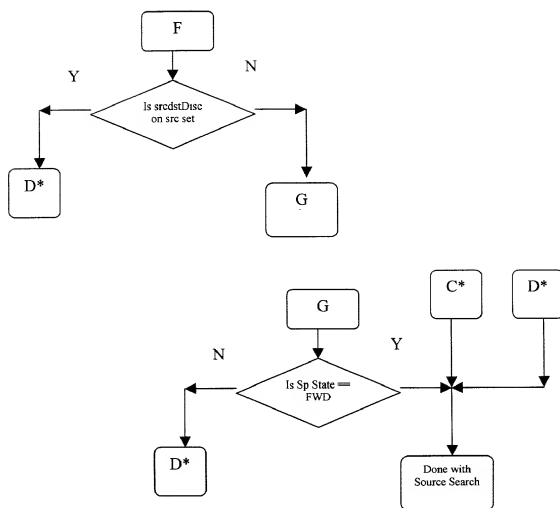


Fig. 7

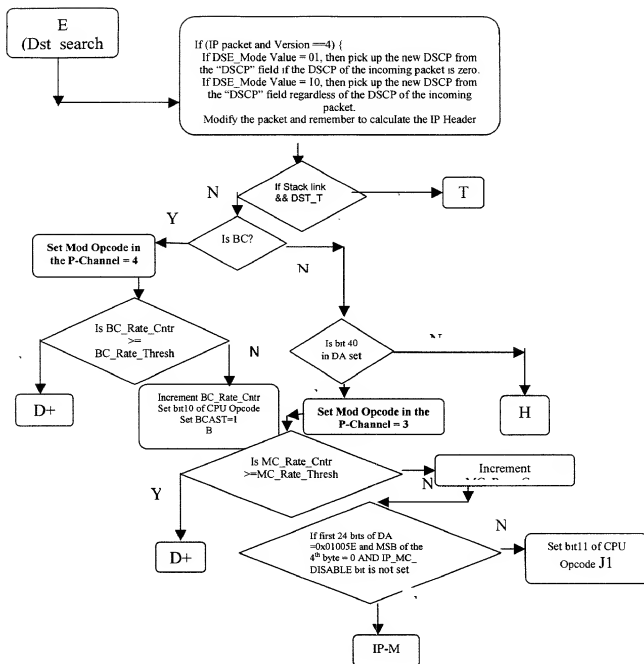


Fig. 8

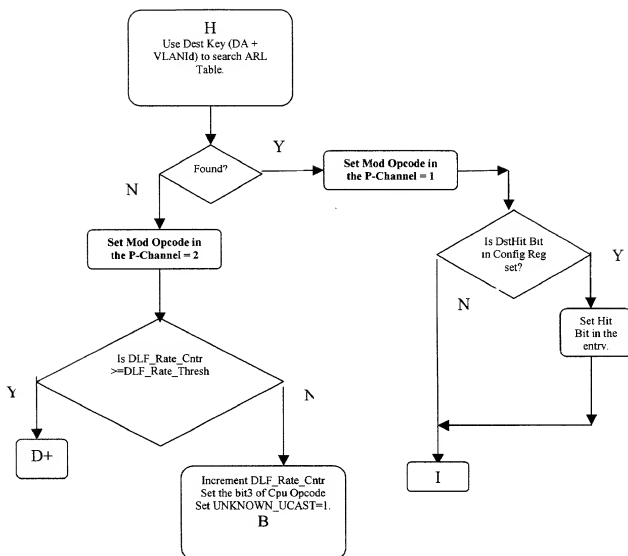


Fig. 9

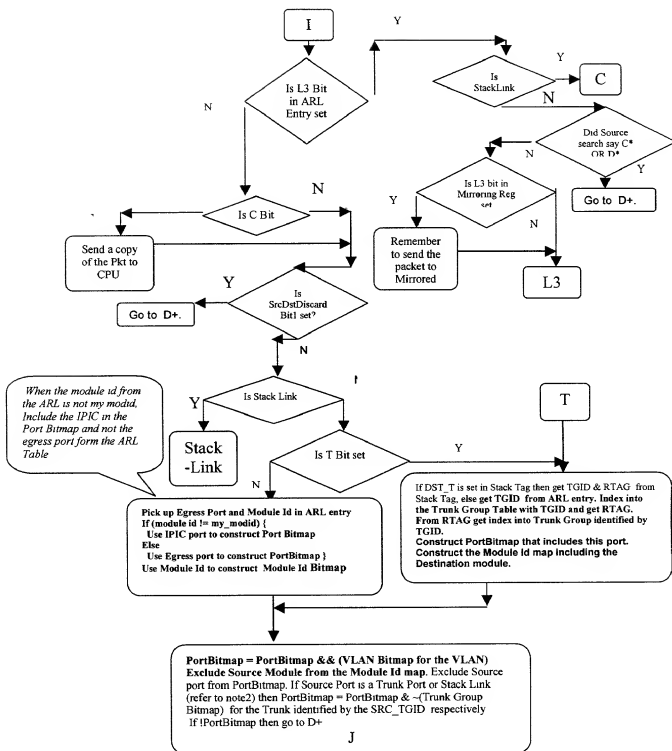


Fig. 10

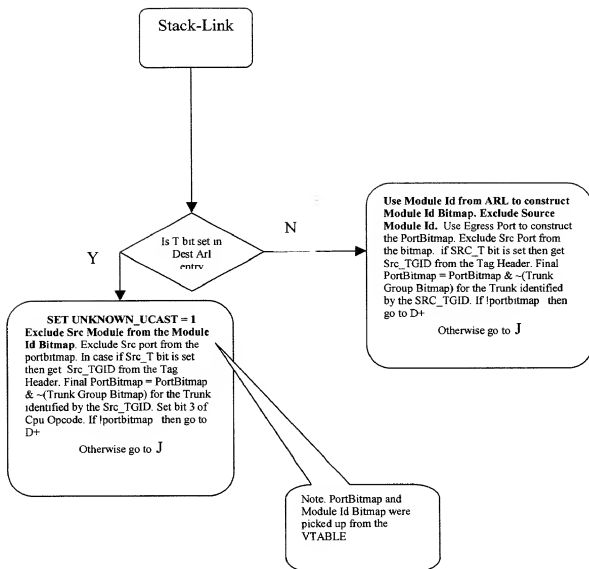


Fig. 11

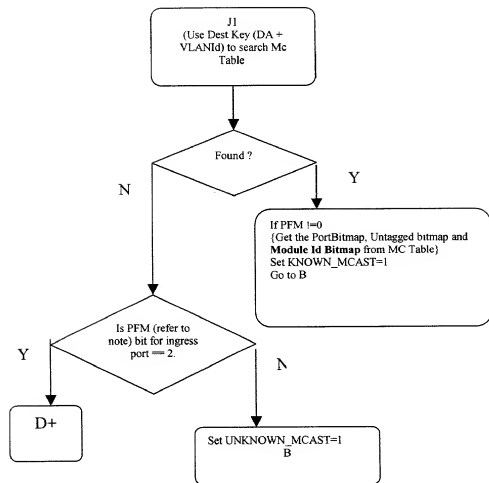


Fig. 12

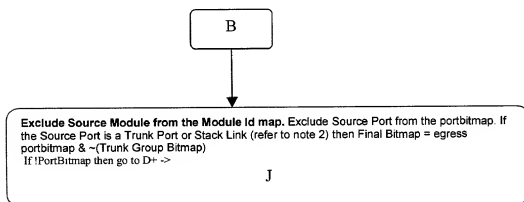


Fig. 13

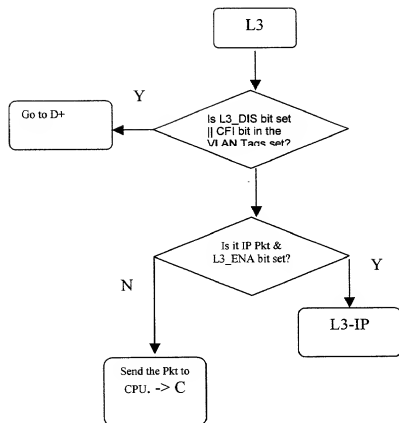


Fig. 14

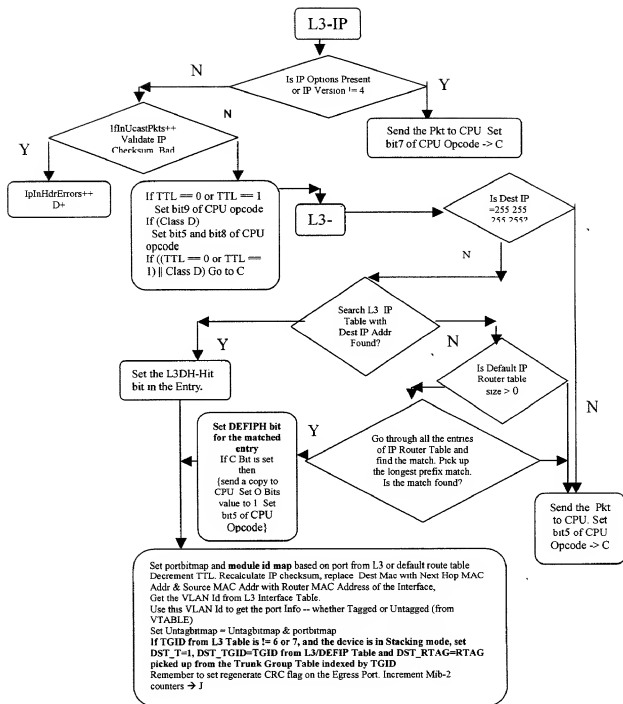


Fig. 15

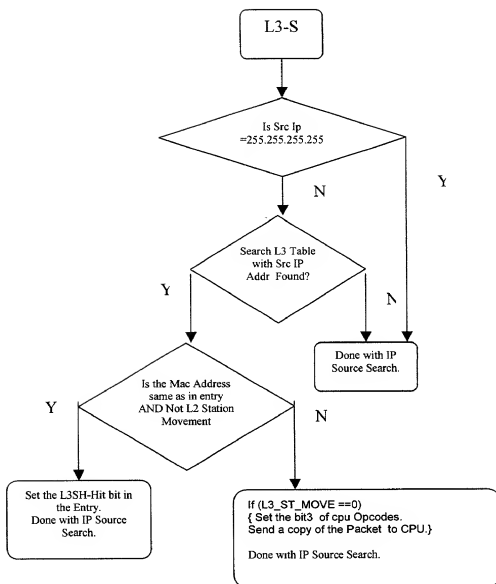


Fig. 16

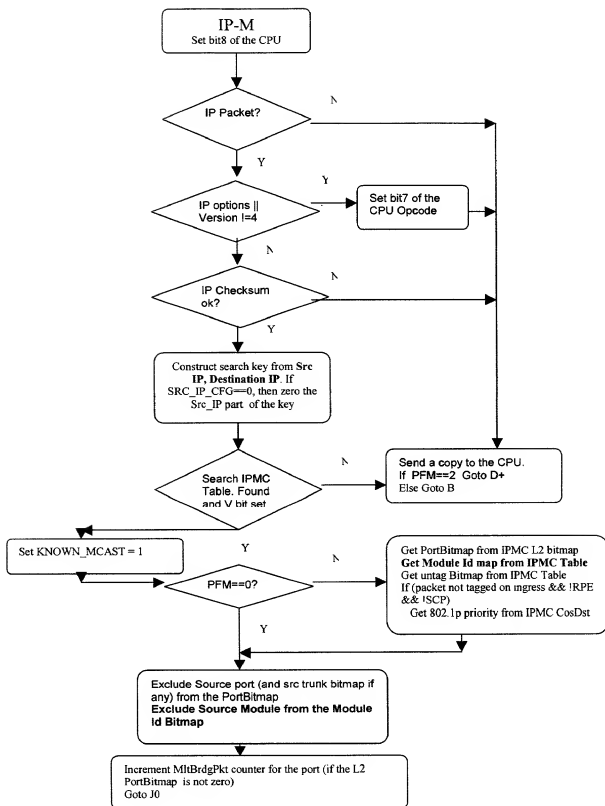


Fig. 17

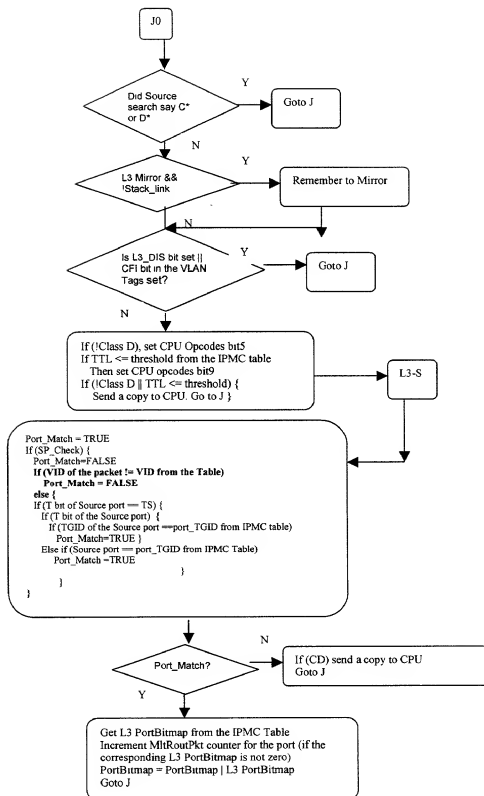


Fig. 18

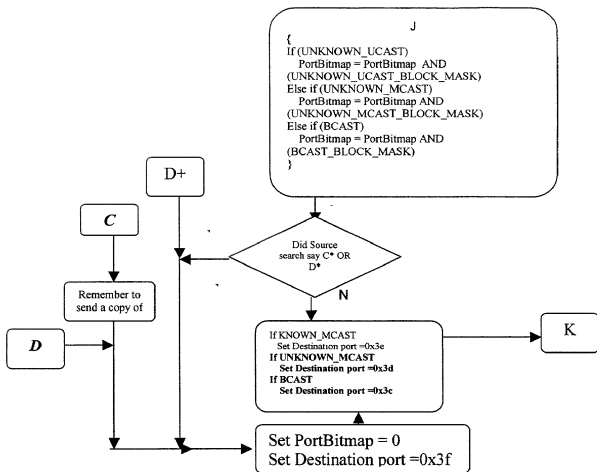


Fig. 19

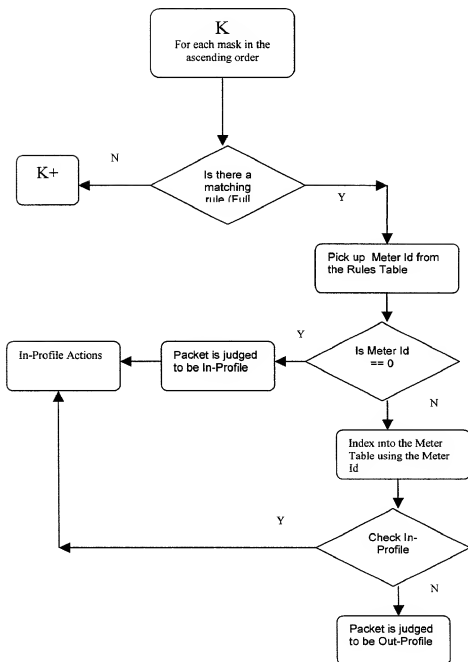


Fig. 20

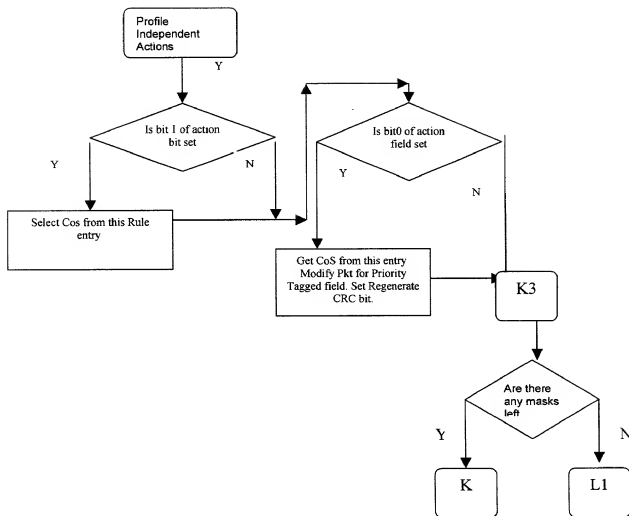


Fig. 21

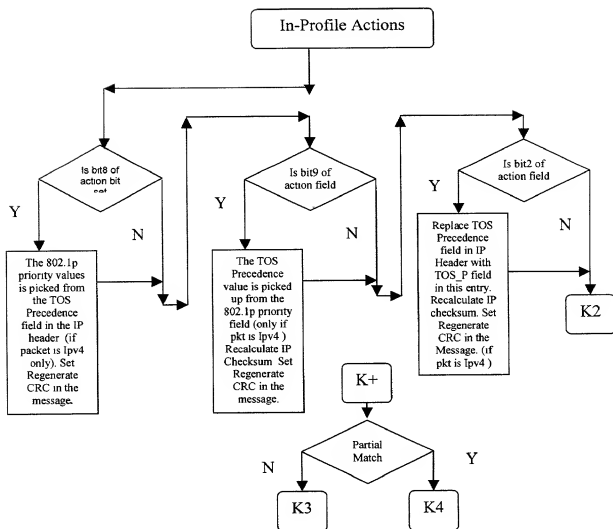


Fig. 22

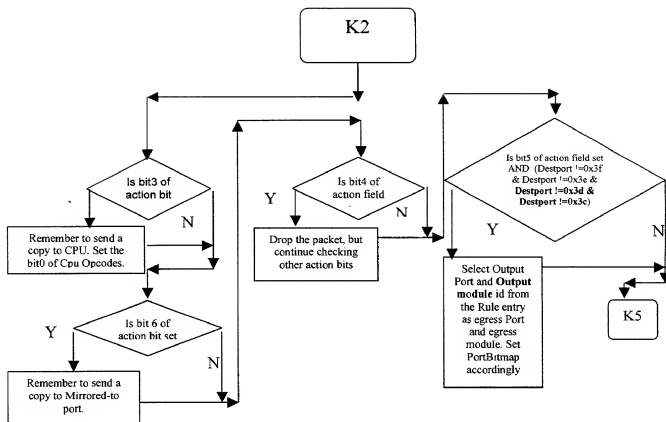


Fig. 23

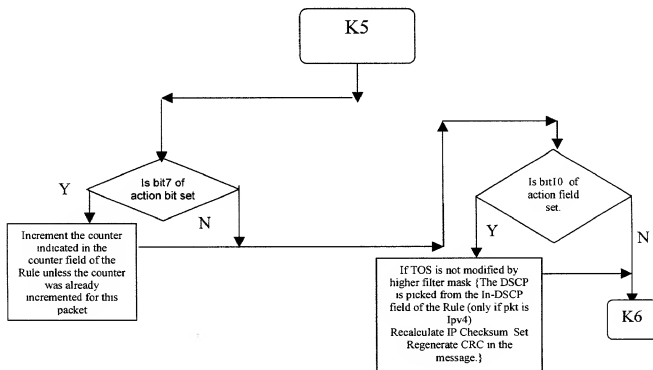


Fig. 24

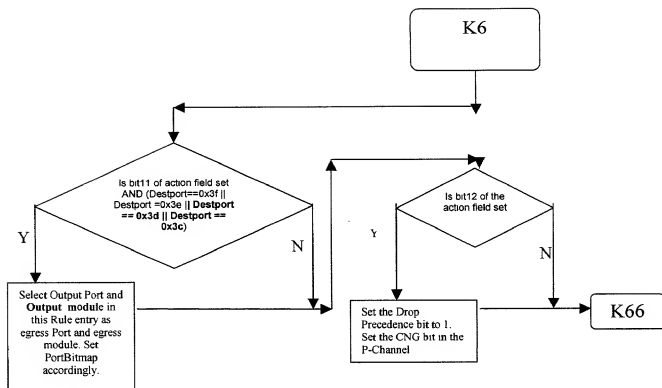


Fig. 25

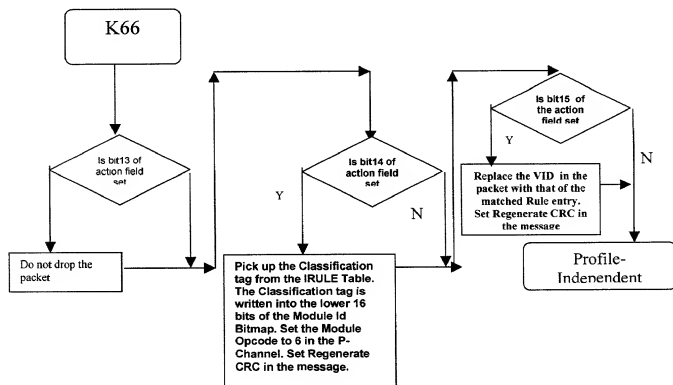


Fig. 26

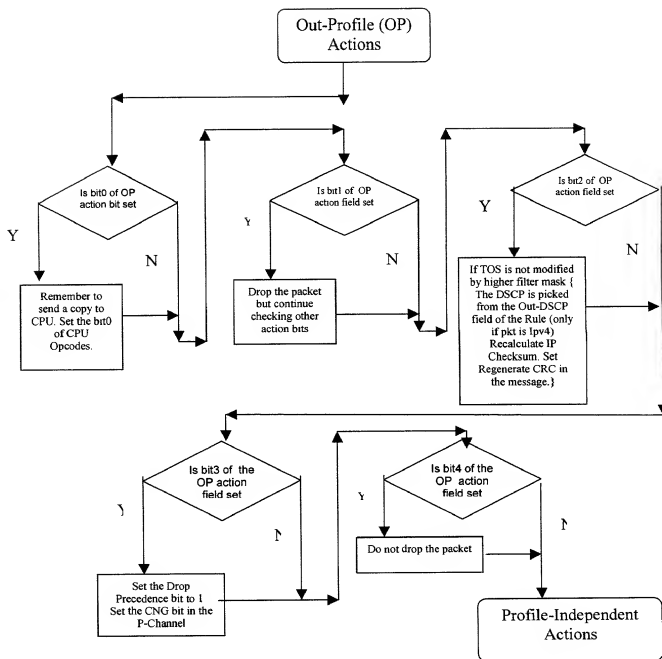


Fig. 27

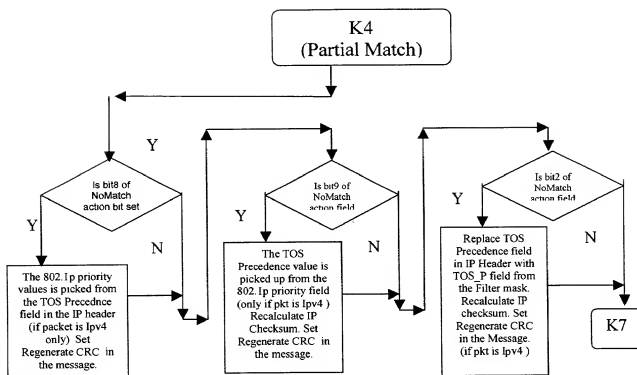


Fig. 28

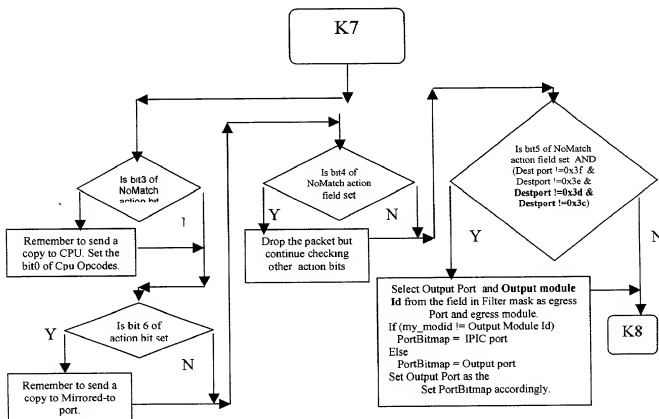


Fig. 29

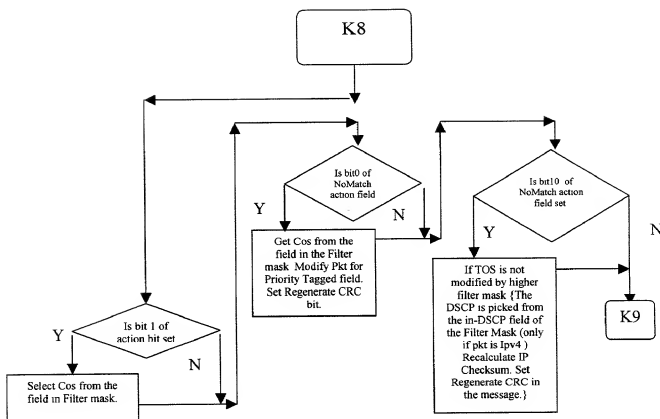


Fig. 30

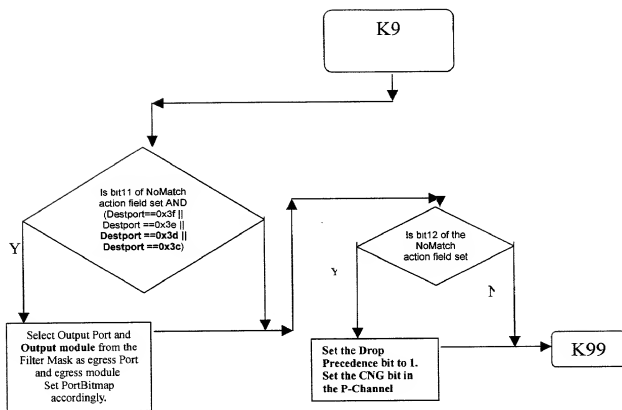


Fig. 31

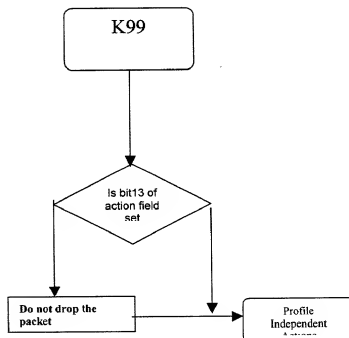


Fig. 32

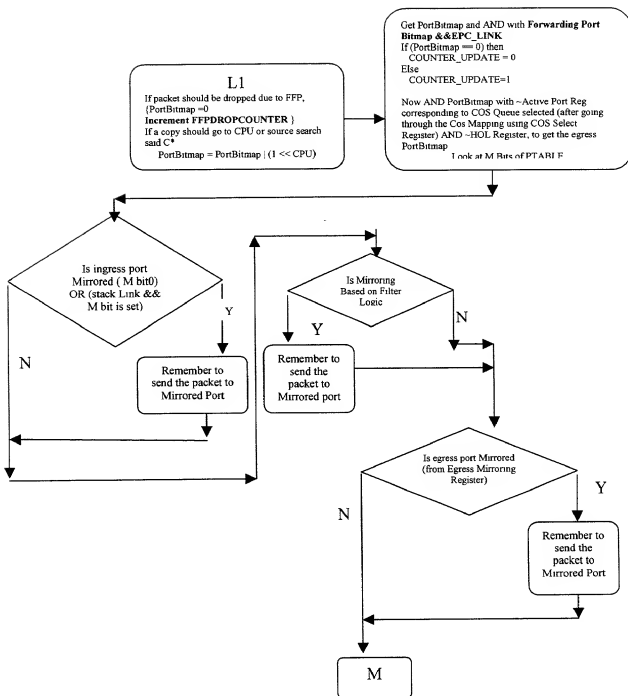


Fig. 33

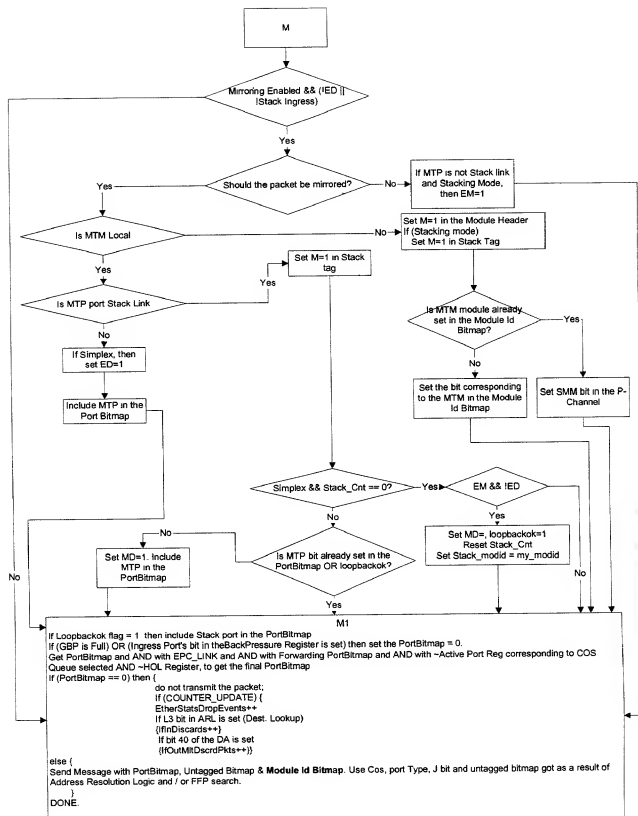


Fig. 34

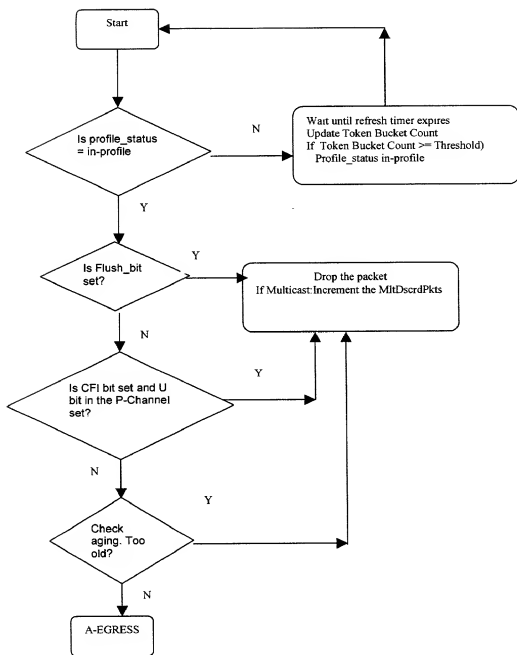


Fig. 35

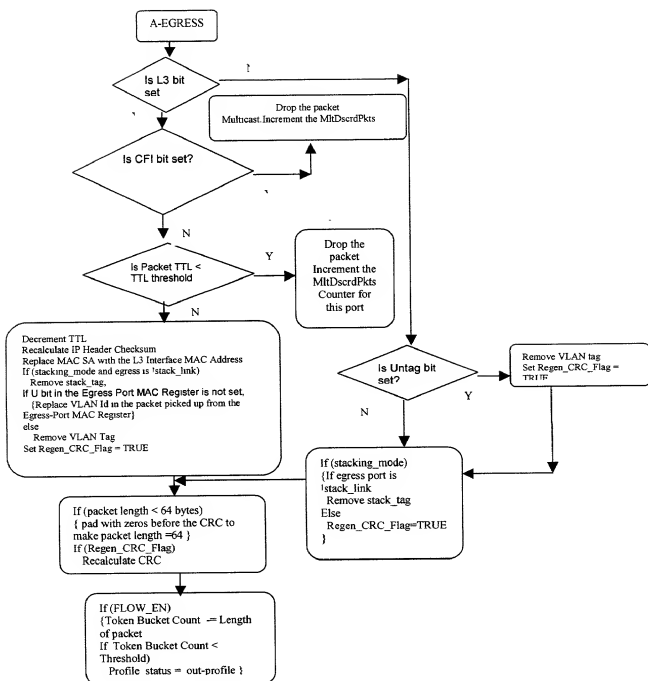


Fig. 36

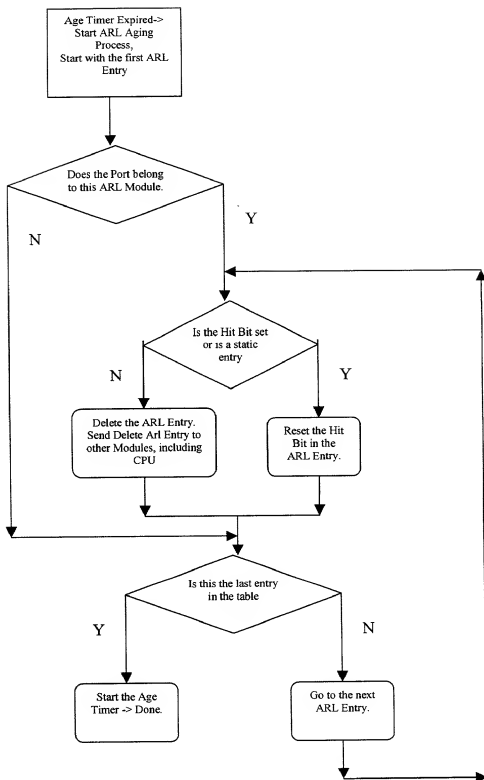


Fig. 37

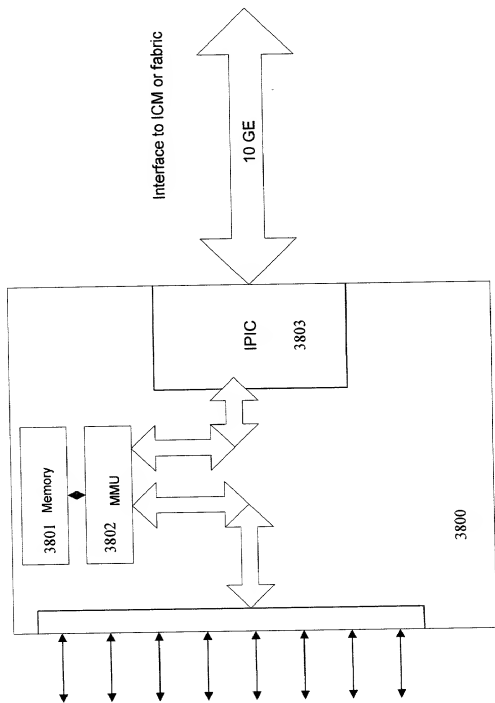


Fig. 38

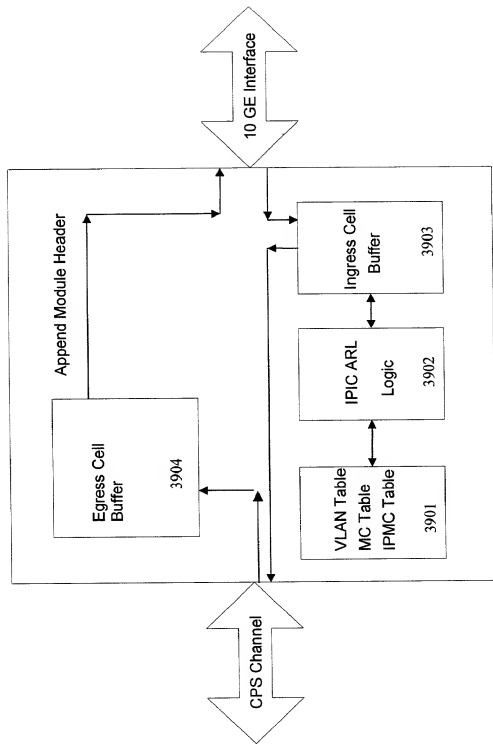


Fig. 39

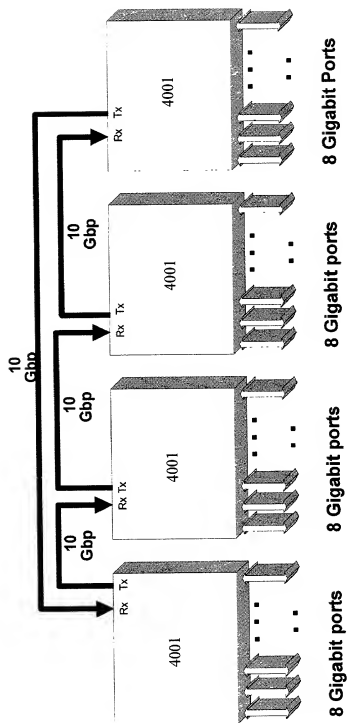


Fig. 40

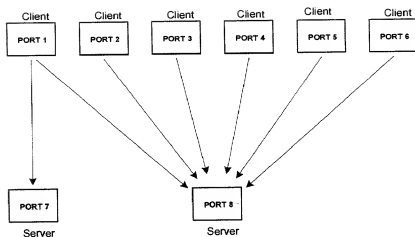


Fig. 41

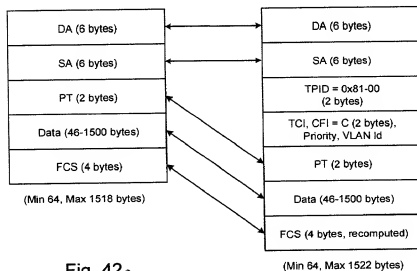


Fig. 42a

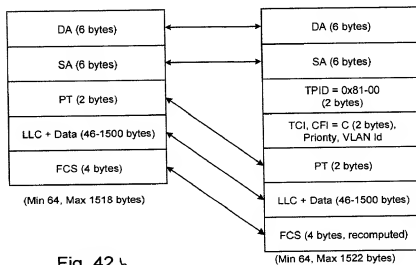


Fig. 42b

09877022.061101
T01190*2202266

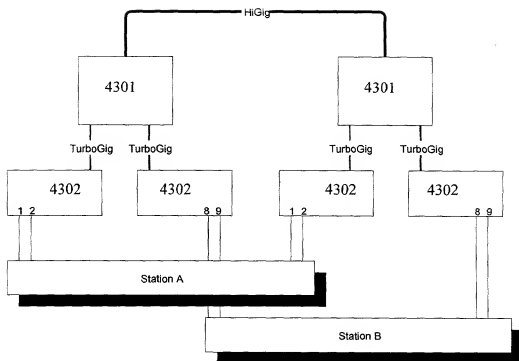


Fig. 43

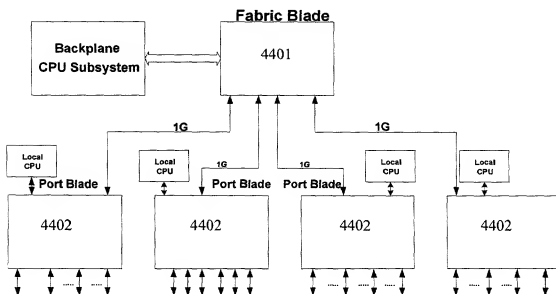


Fig. 44

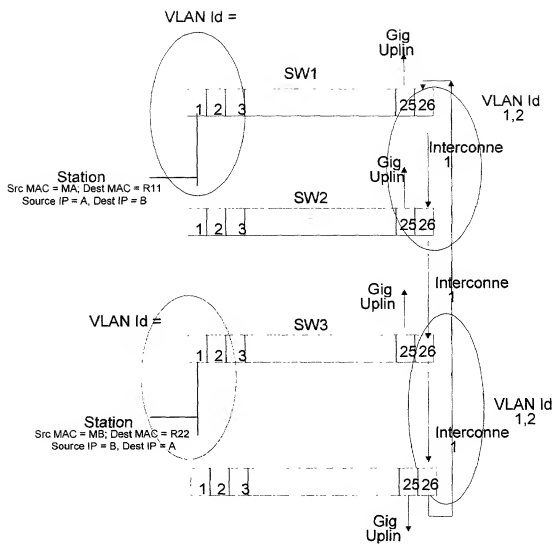


Fig. 45

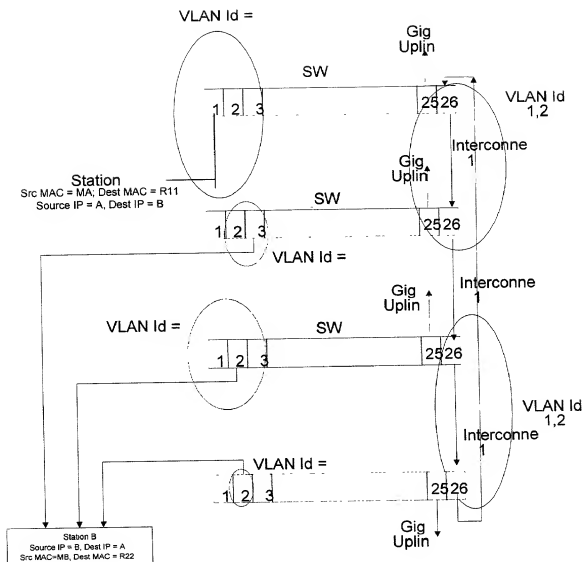


Fig. 46